In the Specification:

In the title:

Please delete the current Title and substitute the following therefor: -PASSENGER TRANSIT CAR INCLUDING A SELF-LOCKING MEMORY OR BUS HOLD CIRCUIT FOR A TRISTATE DATA BUS-.

In the Abstract:

Please delete the current Abstract and substitute the following therefor:

A passenger transit car such as a rail car including a self-locking memory circuit for a tristate data bus having multiple bit lines. ~~The self-locking circuit is located on a printed circuit board that is directly connected a mother board which, in turn, is directly connected to motors, solenoids and switches which couple considerably more electrical noise onto the data lines and the self-locking circuit than the electrical noise present in conventional environments for self-locking circuits.~~ The circuit includes a non-inverting amplifier chip for connection to one of the bit lines and a resistor having a predetermined electrical resistance connected across the amplifier chip. The chip and resistor provide a predetermined impedance ~~to the flow of electrical current~~ in the self-locking circuit to reduce the effects of electrical noise on the data bus

which can be considerable due to motors, solenoids and switches in the passenger transit car. The circuit changes its state when the current of the latest information on a bit line builds or lowers above or below the upper and lower threshold levels of the self-locking circuit. ~~The tristate data bus may be connected between a digital signal processor (DSP), a complex programmable logic device (CPLD) and a central processing unit (CPU) operating at different rates or speeds.~~

In the Brief Description of the Presently Preferred Embodiment:

Please delete the paragraph bridging pages 6 and 7 and substitute the following therefor:

Reference is now made, more particularly, to the drawings. Figures 1A and 1B together show eight buffer memory circuits, generally designated 220, electrically connected, respectively, to eight tristate bit lines 0 through 7 of a data bus 9 interconnected between transceiving digital components 20 and 30. An example of such an interconnection of components is the central processing unit (or "CPU") 230, the Motion Control Digital Signal Processor (or "DSP") in block 320 and the 300 Complex Programmable Logic Device (or "CPLD") also in block 320 ~~300~~ interconnected in the read/write manner shown in Figures 5B and 8B of the above incorporated provisional patent application.

F2

Please delete the second full paragraph on page 13 and substitute the following therefor:

F3

Specifically, as shown in Figure 4, each door operator 40 is deployed with one or more door lock solenoids 34 and a side select emergency lockout solenoid 36, both controllable by the DCU 74 in response to the side select signal. Additional outputs are the lock 38 and unlock 40 for the cliff/side lockout, a close confirmation interlock solenoid 42 and a warning lamp/fault indicator 44.

Please delete the second full paragraph on page 14 and substitute the following therefor:

F4

Illustrated in Figures 4 and 5 are the essential details of an intelligent door controller unit (IDCU) 150 and related inventions. The IDCU is preferably organized into three modules: a CPU card 200, a motor driver & input/output (MD-I/O) card 300, and a power supply card 400. Each of these cards features a printed circuit board onto which an industry-standard bus structure, such as the PC-104 embedded processor interface, has been laid out. A simplified representation of the bus structure is shown in Figure 5. It is into this bus structure that the addressable components of the invention have been incorporated.

Please delete the paragraph bridging pages 14 and 15 and substitute the following therefor:

F5

Designed to serve as the motherboard for the IDCU 150, the MD-I/O card 300 has upwardly disposed connectors built into its bus structure. Being physically linked to the motherboard via such connectors, the CPU and power supply cards 200 and 400 can thus be stacked horizontally atop the MD-I/O card 300. This allows the IDCU to be contained compactly within a single enclosure. As explained in greater detail below, this modular architecture also allows more capability to be added to the IDCU merely by connecting additional cards to the vertical bus structure by which the desired functions can be implemented.

Please delete the paragraphs beginning with the paragraph bridging pages 15 and 16 through the paragraph bridging pages 21 and 22 and substitute the following therefor:

F6

As best shown in Figures 4 and 5, among other components, the MD-I/O card 300 includes a novel optoisolator device 310, several CPLDs in block 320, a motion control (digital signal) processor 320 (DSP chip) also in block 320, motor current and power monitoring circuitry 326, an H-bridge amplifier 330, a seven segment display 340, and an audio ~~a tone/audio~~ amplifier

350. Three CPLDs in block 320 are critical to the operation of the MD-I/O card 300: the ADD-CPLD 316, the I/O-CPLD including two separate blocks in Figure 4, an I/O input block 312 and an ~~as~~ I/O output block 314, and the MC-CPLD 318. The ADD-CPLD 316 handles the address decoding functions. The I/O-CPLD (312, 314) handles the input and output functions of the IDCU. The MC-CPLD 318, in conjunction with the DSP chip in block 320, handles the motion control functions inclusive of controlling the H-bridge amplifier 330 to drive the motor 76 of the door operator. These CPLDs are preferably in-system-programmable (ISP) devices. Well known in the electronic arts, each CPLD is capable of being programmed/reprogrammed within the bus structure of the circuit into which it has been incorporated. Each CPLD also features in-system diagnostic capabilities, meaning that each is capable of storing data about its own operations and reporting such data to the CPU card 200 when queried for same as part of the diagnostic tests.

The I/O CPLD (312, 314) is the component through which the central command signals and the local door hardware signals are input into the IDCU 150. As can be seen from Figures 4 and 5, the I/O-CPLD (312, 314) chip serves as the interface between the main control components of the IDCU 150 and the CDC 33 of the transit authority. The I/O-CPLD (312, 314) can take the form of the ISP-2064 chip manufactured by the Lattice Semiconductor

Corporation. The IO CPLD block 314 has connected to it an IO output over current protection circuit 370.

The I/O CPLD (312, 314) is preferably deployed with the novel optoisolator device 310, also referred herein as the mirror-image optoisolator circuitry. It is well known, of course, that all of the central command inputs are considered extremely safety critical because a fault anywhere in the input path that these signals follow into a DCU can give ~~cause given~~ rise to serious problems within any door system. The I/O-CPLD (312, 314) and the optoisolator device 310 together serve to monitor and verify the central command signals that the IDCU 150 receives from the CDC 33.

As noted earlier, the IDCU 150 can accept central command signals from either the discrete trainlines 130 (i.e., a hard-wired switch interface) or an optional serial communications link 328. For example, regarding the discrete trainlines 130, the central command inputs can be conveyed to the IDCU 150 via a single-switched or a doubled-switched input format. In the single-switched format, one line is activated and its associated return line (commonly the ground) is hardwired to the CDC. In the doubled-switched format, both the input line and its associated return are activated together at the CDC. When not in use, both lines are shorted together to reduce the chance of

unwanted bias voltages or ground loops from triggering a door control signal.

The optoisolator device 310 optically isolates the IDCU from the discrete trainlines whether conveyed via the single-switched or the doubled-switched input format. It is well known that the discrete trainlines are susceptible to picking up rather high voltage spikes from the environment in which they are used. Transit authorities thus require optical isolation because it protects the IDCU from such high voltage spikes; spikes that could otherwise cause the doors to operate improperly and even damage the electronics. Once the central command inputs are received by the optoisolator device 310, they are clamped and filtered to reduce the possibility of transients from getting into the IDCU 150 via the I/O-CPLD (312, 314). For each input line, an input-voltage decoupler is used to minimize the effects of low-voltage DC bias signals. In addition, the values of the input circuits are tailored to suit the voltage requirements of the train. Furthermore, the line filters are tuned to minimize the electrical noise spectrum expected to be seen by the IDCU.

In addition to monitoring and verifying the authenticity of all trainline inputs, the CPU 200 and I/O-CPLD (312, 314) together route the incoming central command inputs and local door hardware inputs to the appropriate component in the IDCU 150 so that the required task(s) can be performed. The I/O-CPLD (312,

314) is also programmed to handle various output functions for the IDCU 150. The following is merely a brief list of the functions that the I/O-CPLD (312, 314) can be programmed to perform: filter the central command signals received from the trainlines; monitor and decode all central command inputs; detect erroneous signals; generate CPU I/O interrupt signals; monitor various passenger activated switches; control speaker/beepers on MD-I/O card 300; control the warning lamp(s) outside the doorway(s); monitor power-supply voltages; monitor the I/O output fault status; test the optocouplers; test the input and encoder connectors for proper connection; transfer status and interrupt data to the MC-CPLD 318; generate the clock pre-scalar signals; and control one of the two unlock actuators of the two door ~~37~~ lock assemblies.

Still referring ~~Referring now~~ to Figures 4 and 5, the MC-CPLD 318 ~~316~~, in conjunction with the motion control processor (DSP chip) 320, handles the motion control functions inclusive of controlling the H-bridge amplifier 330 to drive the motor 76 of the door operator. The MC-CPLD 318 and the DSP chip 320 can take the form of the ISP-1032 and LM629 chips manufactured by the Lattice Semiconductor Corporation and National Semiconductor Corporation, respectively. Like the aforementioned CPLDs, these chips are commercially available devices. The following specification sheets for these devices are incorporated herein by

reference: ADD-CPLD (ISP22lv_03 sheet dated March 1998), I/O-CPLD (2064_04 sheet dated October 1998) and MC-CPLD (1032_05 sheet dated October 1998) published by Lattice Semiconductor Corporation; and the LM629 chip (TL/H/9219 dated February 1995) published by the National Semiconductor Corporation. The MC-CPLD 318 and various related circuits and components are disposed on the MD-I/O card 300. The output control circuits in the MC-CPLD 318 ~~316~~, as well as those in the I/O-CPLD (312, 314), have built-in short circuit protection, which will shutdown the output operations should a fault be detected. Implemented primarily within the MC-CPLD chip 318 ~~316~~ are the data/address control logic, the current feedback and deadtime circuitry, the encoder monitoring circuitry, and the interrupt control logic. The access key circuitry 322, the watchdog timer circuitry 324 and the motor control circuitry for the H-bridge 330 ~~230~~, shown in Figures 4 and 5, are implemented both internal and external to the MC-CPLD 318. The integration capacitor circuitry 325 is external to the MC-CPLD 318, as is best shown in Figure 5. This circuitry is used to monitor the power/wattage in the motor 76 during overload conditions, otherwise it is discharged.

Regarding the motion control processor 321 ~~320~~, the LM629 chip was selected for the control of the motor. This chip was designed to operate in a stand-alone mode of operation where there are no supporting RAM or ROM chips for the DSP low level

program. This makes the DSP chip nearly impervious to internal crashes and, although it is a complex 32 bit device, it has an inherent ruggedness that is not surpassed with any other device. It is well suited to electrically noisy environments where safety is the utmost consideration. This chip also is capable of serving as a component common to a variety of different door control system architectures. This is possible due to the tremendous amount of control range built into the DSP chip in block 320.

The LM629 is preferred because it lends itself to a motor control design that is almost entirely digital in operation. Because no analog control loops are used (e.g., linear current & tachometer feedback), the IDCU 150 is relatively immune to noise causing position/velocity errors in the operation of the doors.

Figures 4 and 5 best illustrate the H-bridge amplifier 330. Driven by the motor current circuitry in the MC-CPLD via pwm and direction signals, the H-bridge amplifier 330 includes optical isolation circuitry 360, level shifting circuitry 362, and field effect transistors (FETs) 364 with which to drive the motor. ~~The lower two FETs are current sensing devices. They provide to the motor current and power monitoring circuitry 326 in the MC-CPLD feedback as to the magnitude of the current in the motor 76. This analog feedback 366 is used only to protect the H-bridge circuitry 330 and the motor 76 during dynamic braking.~~ The IDCU

does not use current feedback to detect obstructions. Circuitry is also employed to protect the components of the H-bridge circuitry 330 and the motor 76 from surge voltages and other adverse electrical influences. An encoder 368 provides digital feedback to the MC-CPLD 318.

The IDCU 150 also makes use of four limit switches to help qualify the real position of the doors. These switches are ~~best~~ shown in Figure 4 ~~Figures 4 and 5~~. These switches include (1) two door close limit switches (one per door panel) 616 showing the doors are in the closed position ~~616~~; (2) two pushback lock switches 58 each indicating that its lock member is partially engaged, i.e., in the pushback-locked state; (3) two full lock switches 56 each indicating that its lock member is fully engaged, i.e., in the fully-locked state. In this state, the full lock switches indicating to the IDCU that the power need no longer be supplied to the motor 76. Other inputs to the IDCU are push back position switches 340, external and internal emergency door release switches 342 and 344, respectively, and a passenger door hold/open push button switch 346.